

1-Mbit (128K x 8) Static RAM

Features

- Pin- and function-compatible with CY7C1018CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low Active Power
 - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS Standby Power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Center power/ground pinout
- Easy memory expansion with \overline{CE} and \overline{OE} options
- Available in Pb-free 32-pin 300-Mil wide Molded SOJ

Functional Description^[1]

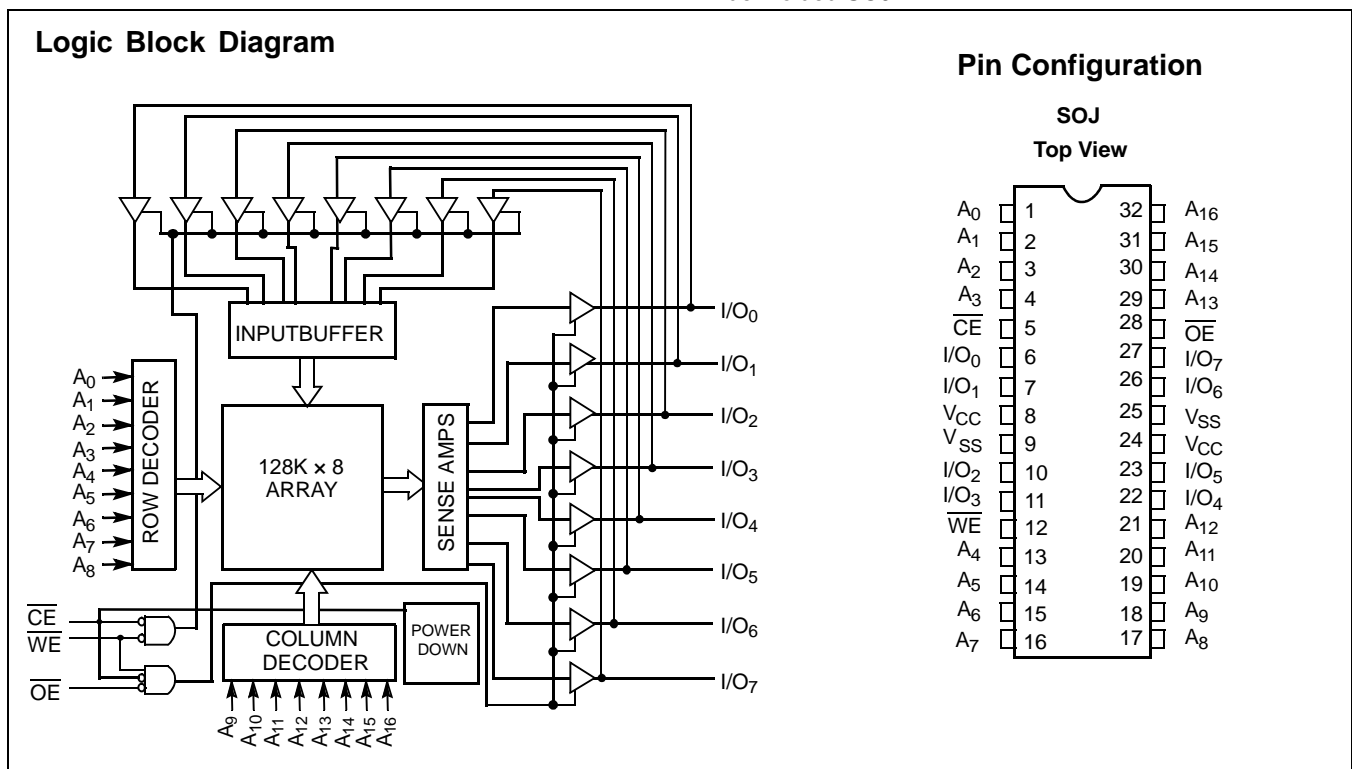
The CY7C1018DV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1018DV33 is available in Pb-free 32-pin 300-Mil wide Molded SOJ.



Note

1. For guidelines on SRAM system designs, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Selection Guide

	-10 (Industrial)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	60	mA
Maximum Standby Current	3	mA

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[2] ... -0.3V to + 4.6V
 DC Voltage Applied to Outputs^[2] in High-Z State -0.3V to V_{CC} + 0.3V

DC Input Voltage^[2] -0.3V to V_{CC} + 0.3V
 Current into Outputs (LOW) 20 mA
 Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40°C to +85°C	3.3V ± 0.3V	10 ns

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10 (Industrial)		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	100MHz	60	mA
			83MHz	55	mA
			66MHz	45	mA
			40MHz	30	mA
I _{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		10	mA
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		3	mA

Note
 2. V_{IL} (min.) = -2.0V and V_{IH}(max) = V_{CC} + 1V for pulse durations of less than 5 ns.

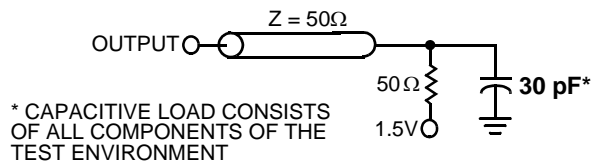
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	8	pF
C _{OUT}	Output Capacitance		8	pF

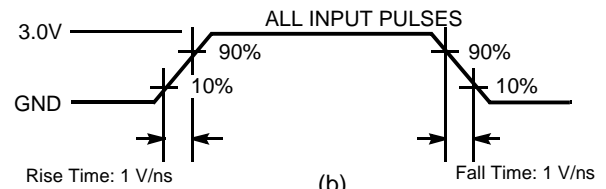
Thermal Resistance^[3]

Parameter	Description	Test Conditions	400-Mil Wide SOJ	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	57.61	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		40.53	°C/W

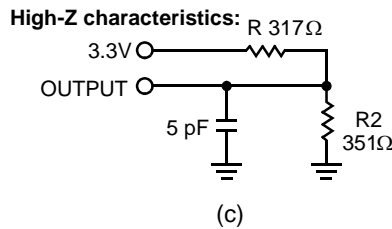
AC Test Loads and Waveforms^[4]



(a)



(b)



(c)

Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

AC Switching Characteristics Over the Operating Range ^[5]

Parameter	Description	-10 (Industrial)		Unit
		Min.	Max.	
Read Cycle				
$t_{\text{power}}^{[6]}$	V_{CC} (typical) to the first access	100		μs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		10	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low-Z	0		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High-Z ^[7, 8]		5	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low-Z ^[8]	3		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High-Z ^[7, 8]		5	ns
$t_{\text{PU}}^{[9]}$	$\overline{\text{CE}}$ LOW to Power-up	0		ns
$t_{\text{PD}}^{[9]}$	$\overline{\text{CE}}$ HIGH to Power-down		10	ns
Write Cycle^[10, 11]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	8		ns
t_{AW}	Address Set-up to Write End	8		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	7		ns
t_{SD}	Data Set-up to Write End	5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low-Z ^[8]	3		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High-Z ^[7, 8]		5	ns

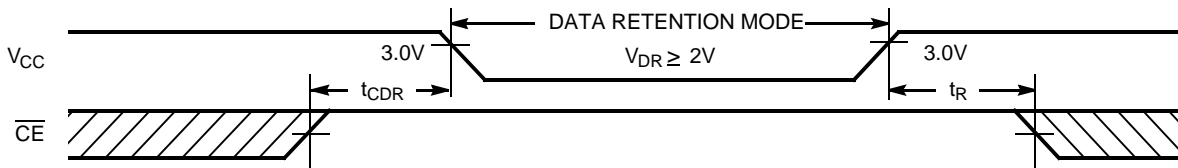
Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. This parameter is guaranteed by design and is not tested.
10. The internal Write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics (Over the Operating Range)

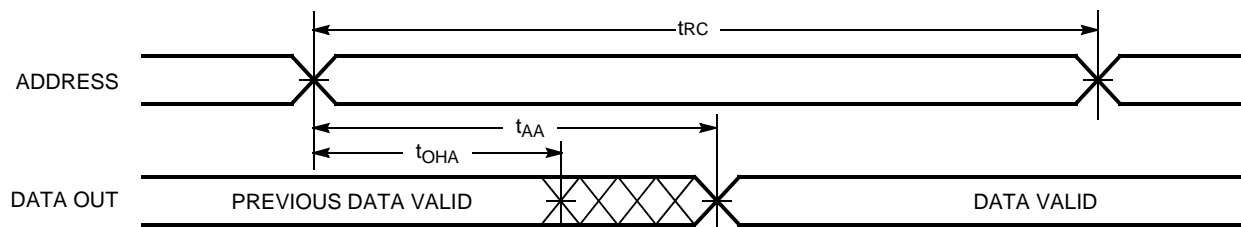
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V, \overline{CE} \geq V_{CC} - 0.3V, V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		3	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[12]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

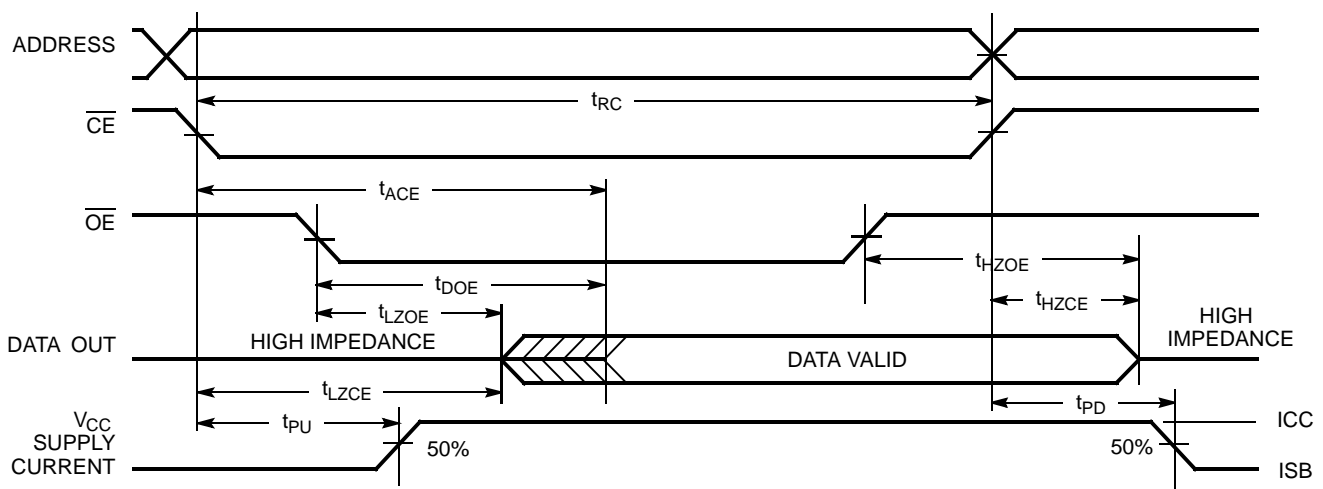


Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[13, 14]



Read Cycle No. 2 (\overline{OE} Controlled)^[14, 15]

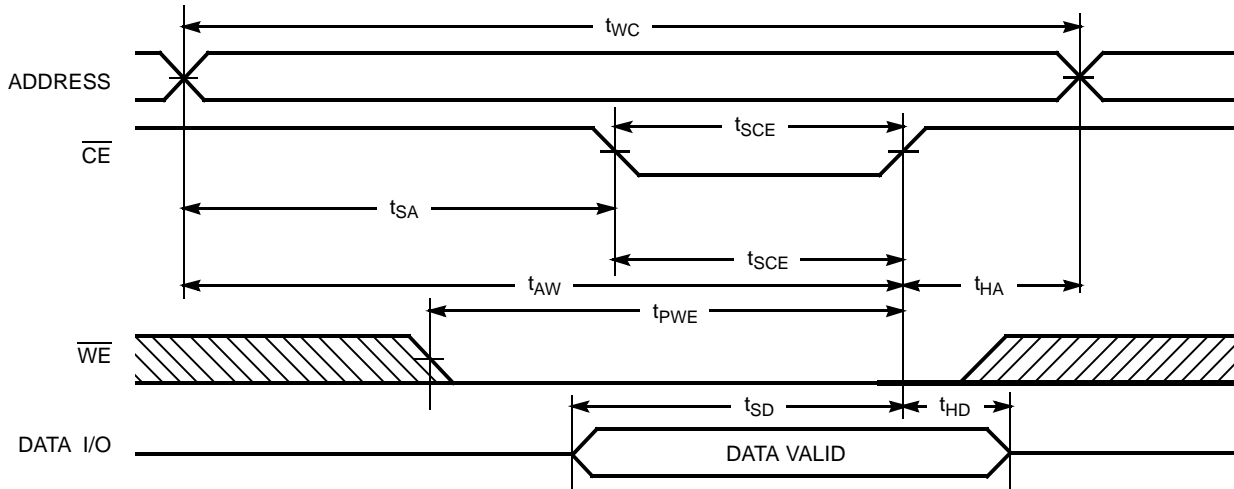


Notes

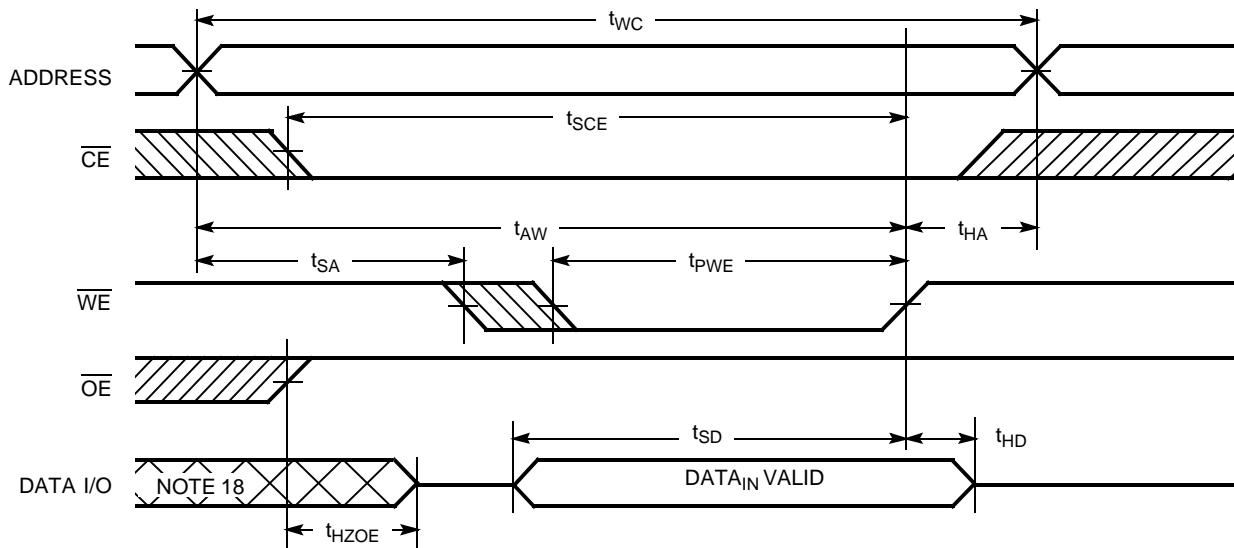
- 12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50 \mu s$ or stable at $V_{CC(min.)} \geq 50 \mu s$.
- 13. Device is continuously selected. $OE, CE = V_{IL}$.
- 14. WE is HIGH for Read cycle.
- 15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[16, 17]



Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[16, 17]

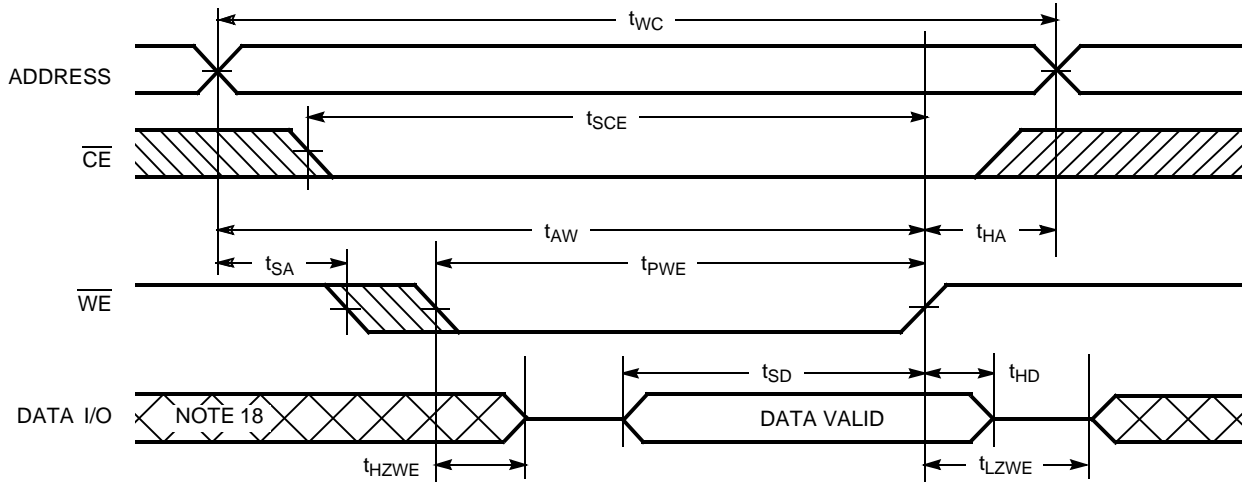


Notes

- 16. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
- 18. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[11, 17]



Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

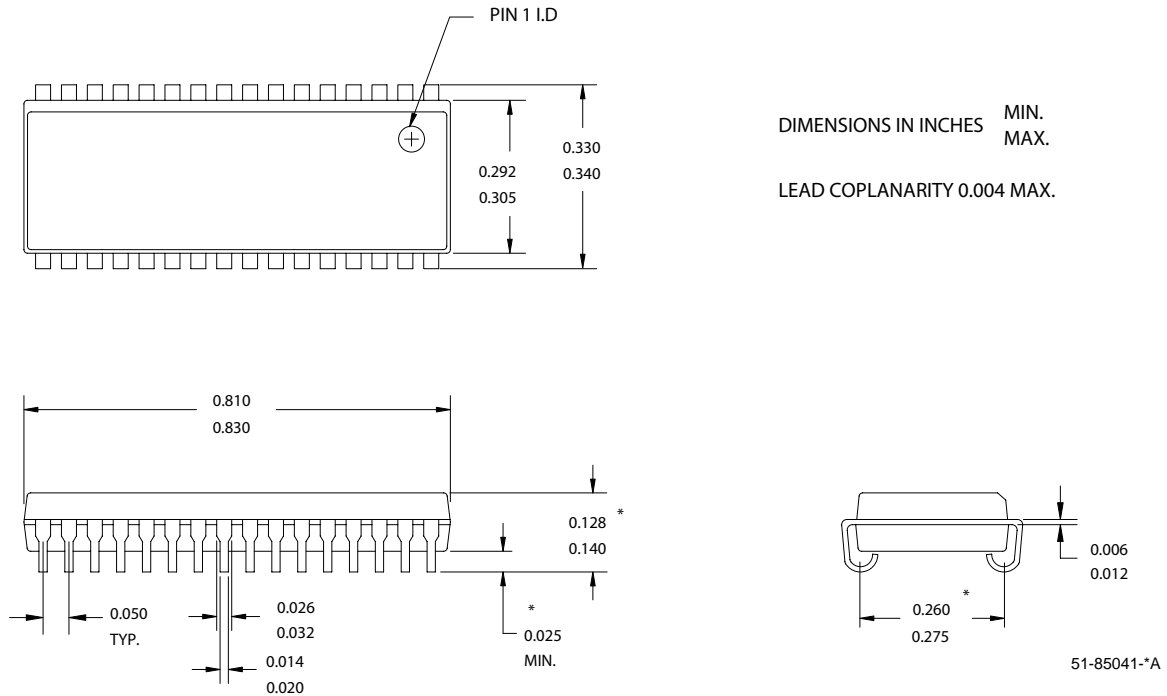
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1018DV33-10VXI	51-85041	32-pin (300-Mil) Molded SOJ (Pb-free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

Package Diagram

Figure 1. 32-pin (300-Mil) Molded SOJ (51-85041)



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Document History Page

Document Title: CY7C1018DV33, 1-Mbit (128K x 8) Static RAM Document Number: 38-05465				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	238471	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in the Ordering Information
*B	262950	See ECN	RKF	Added Data Retention Characteristics table Added T _{power} Spec in Switching Characteristics table Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -8 and -10 ns
*D	520647	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 8 ns speed bin Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #2